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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/520,653	01/10/2005	Yuki Kondoh	XA-10256	5188

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
CARDWELL, ERIC	
ART UNIT	**PAPER NUMBER**
2112	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/21/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/520,653	KONDOH ET AL.	
	Examiner	Art Unit	
	Eric S. Cardwell	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *September 30, 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 12-18* is/are rejected.

7)☒ Claim(s) *3-11,and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/30/2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/10/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 2, are rejected under 35 U.S.C. 102(b) as being anticipated by Biggs [5,410,669]. Biggs teaches a method of data processing having a dual-purpose memory comprising multiple cache sets.

Regarding claim 1, Biggs teaches the uses of a first memory [figure 1, feature 16] that is cache memory, a second memory [figure 1, feature 14] that can either be cacheable or non-cacheable [column 3, lines 2-4] and a read buffer capable of input/output control [figure 1, feature 18].

Regarding claim 2, Biggs teaches the use of a controller [figure 1, feature18], controllers have registers for holding address and predetermined access data. Controllers by their nature facilitate the input and output from the caches.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 12-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Biggs et al. [5,410,669], in view of Kumar [6,678,790]. Biggs teaches a method of data processing having a dual-purpose memory comprising multiple cache sets. Kumar teaches an integrated circuit having a memory, which is reconfigurable as a main memory or as a cache memory.

Regarding claim 12, Biggs teaches the use of a first memory constituting a cache memory [figure 1, feature 16]. However, Biggs does not teach the use of a secondary memory that can be either cache or RAM.

Kumar teaches a method of reconfigurable memory that can be designated as either cache or RAM [figure 1(a), feature 12 and column 3, lines 20-27]. Kumar also uses a control register for setting which type of memory will be used [figure 1(a), feature 16]. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to combine Biggs and Kumar inventions because of the space requirement issues in semiconductor devices, that if one wanted to add main memory onto the device the space may not be available to do so, but one could take advantage

of the space already in place by the secondary cache and use it as main memory via Kumar's method.

Regarding claims 13 and 14, Biggs teaches a secondary cache controller [figure 3, feature 56]. Biggs also teaches an internal memory controller for controlling the memory that is not cache memory [figure 1, feature 18].

Regarding claim 15, Biggs does not teach the use of a designating means via a control register. However, Kumar does use a control register for setting which type of memory will be used [figure 1(a), feature 16]. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to use Kumar's control register because it would have simplified the designating means of the memory.

Regarding claim 16, Biggs does not teach the reconfigurable secondary memory. However, Kumar's method when combined with Biggs can change cache to RAM. By definition RAM contains addresses that are not cacheable [abstract]. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to combine Biggs and Kumar inventions because Kumar's method would allow for a secondary memory to be cacheable and non-cacheable.

Regarding claims 17 and 18, Biggs does not teach the use of a read buffer. However, Kumar teaches the use of a read buffer [figure 2, feature 20]. The read buffer contains data, and addresses depending on how it is accessed [column 3, lines 60-67 and column 4, lines 13-24]. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to use Kumar's read buffer to output data and hold addresses when the memory is accessed in a non-cacheable way, because

the read buffer would speed up the time it takes to read from the non-cacheable memory.

Allowable Subject Matter

Claims 3-11, and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 3, prior art does not disclose parallel access only serial access.

Regarding claim 4, prior art does not have a read buffer that transfers data from the first memory over the second bus.

Regarding claim 5, prior art does not disclose the use of sequential access buses.

Regarding claim 6, prior art does not teach a third bus connecting the first and second memories.

Regarding claim 7, prior art does not disclose a peripheral bus interface controller connected to the third bus.

Regarding claim 8, prior art does not disclose an internal memory controller connected to the second and third buses.

Regarding claim 9, prior art does not disclose a secondary memory controller connected to the third bus.

Regarding claim 10, prior art does not disclose a method of invalidating memory.

Regarding claim 11, prior art does not disclose a method for setting a control register for the internal and secondary memory controllers.

Regarding claim 19, prior art does not disclose a read buffer connected to a second bus with a greater bus width than a width of the first bus.

Conclusion

Prior art cited but not used:

Anand, Vishai [US 6,134,641] "Method of an system for allowing a computer system to access cachable memory in a non-cacheable manner", Teaches cacheable and non-cacheable memory.

Koga, Manabu [US 2002/0029322] "Microcomputer", teaches a third bus in a similar layout,

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric S. Cardwell whose telephone number is 571-270-1379. The examiner can normally be reached on Mon-Fri 8am-5pm Eastern Alt. Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Walter Griffin can be reached on 571-272-1447. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ESC

WALTER D. GRIFFIN
SUPERVISORY PATENT EXAMINER